首届(西湖)半导体集成电路技术论坛（1st Semiconductor Integrated Circuits Technology Workshop at West Lake，简称SICTW）将于 11 月 6 日-11 月 9 日在美丽的杭州西子湖畔浙江大学玉泉校区举行，本次研讨会将由浙江大学信息与电子工程学院、微电子学院和工程师学院联合举办。我们有幸邀请到了美国Intel公司、美国应用材料公司、美国IBM公司、韩国三星，法国意法半导体公司、灿芯创智微电子公司、 华为等国际行业巨头的高级研发人员或资深研究员 ,以及美国斯坦福大学、卡耐基梅隆大学、德州大学奥斯汀分校、格拉斯哥大学等世界知名学府的高级科研人员主讲，参会的人员规模预计为 250 人左右，其中 100 人为国内高校和研究所的师生，另外的约 150 位名额面向国内主要半导体制造，产品和IP设计企业，EDA与设备制造和材料供应公司开放。因此本次论坛的出席者将覆盖国内主要的集成电路行业高端研发和研究群体，预计将产生一定的影响力，同时为国家培养集成电路高端人才起到一定的推动作用。此外，鉴于最近几年中国集成电路研发的重点是 14nm和 7nm技术的推进，本年度论坛的主题将覆盖 14nm和 7nm技术相关的主要问题，助力增强中国在高端集成电路制造工艺方面的国际领导力。具体的会议和报告信息请见附件。同时，您也可在论坛的网站（http://www.sictw.org）浏览关于注册等更详细信息。

我们热诚期待贵单位的相关研究人员,教师与学生的积极参与。

谨祝 身体健康工作顺利

SICTW 组委会

2017 年 9 月 29 日

# Semiconductor Integrated Circuits Technology Workshop at West Lake (Nov. 6 - Nov. 9, 2017)

**SICTW Committee**

# SICTW Program (November 6th)

- Opening (8:30am – 8:45am) – Workshop organizer
- Welcome speech by high level university official (8:45am to 9:00am) - TBD
- Welcome speech by government official (9:00am to 9:15am) - TBD
- **"On to the Next Fifty Years – Guideposts from the Past Fifty Years"**(9:15am – 10:30am) - *Professor H.-S. Philip Wong*, Willard R. and Inez Kerr Bell Professor, Department of Electrical Engineering and Stanford SystemX Alliance, Stanford University (Presentation 1.1)
- Break(15 minutes)
- **"China's IC Industry: Current State, Environment and Opportunities During Post Moor's Era"** (10:45am-12:15pm) - *Dr. Hanming Wu*, CEO of Bright IP and SMIC consultant (Presentation 1.2)
- Group pictures (12:15pm-12:45pm)
- Lunch (12:45pm-1:45pm)
- **"Nanometer IC Design and Process Technology Co-Optimzations – Challenges and Practices"**(1:45pm-4:45pm) – *Professor David Pan*, Engineering Foundation Endowed Professor, Department of Electrical and Computer Engineering, University of Texas at Austin (Presentation 1.3)

# SICTW Program (November 7th)

- **"Advanced Lithography and Patterning Technologies For and Beyond 5nm"** (8:30am-10:30am) – *Dr. Yan Borodovsky,* Former Intel Sr. Fellow and director of Lithography (Presentation 2.1)
- Break (15 minutes)
- **"Reaching for the N3XT 1,000× of Computing Energy Efficiency"** (10:45am-12:30pm) - *Professor H.-S. Philip Wong*, Willard R. and Inez Kerr Bell Professor, Department of Electrical Engineering and Stanford SystemX Alliance, Stanford University (Presentation 2.2)
- Lunch (12:30pm-1:45pm)
- **"Time-to-Market Minimization for New Product Introductionin Leading Edge Technology Nodes"** (1:45pm-3:45pm) – *Professor Andrzej J. Strojwas*, Joseph F. & Nancy Keithley Professor of Electrical & Computer Engineering, Carnegie Mellon University and Chief Technologist, PDF Solutions, Inc. (Presentation 2.3)
- Social outing on scenic West Lake (4:00pm-6:pm)

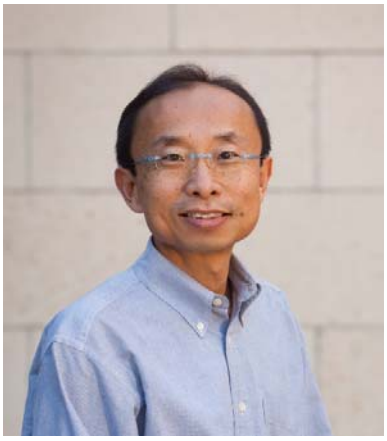
# SICTW Program (November 8th)

- **"Computational Imaging: Scaling Walls"** (8:30am-10:30am) – Dr. Vivek Singh, Intel Fellow and director of computational imaging (Presentation 3.1)
- Break (15 minutes)
- **"Is the FINFET finished?-- Challenges of 10 nm and 7 nm FINFET for Server and Mobile Applications"** (10:45am-12:45pm) – *Dr. Rama Divakaruni*, IBM Distinguished Engineer, IBM Advanced Process Technology Research (Presentation 3.2)
- Lunch (12:45pm-2:00pm)
- **"Interconnect - the Past, the Present and the Future"** (2:00pm-3:45pm) – *Dr. Mehul Naik*, Principal Member of Technical Staff, Applied Materials (Presentation 3.3)
- Break (15 minutes)
- **"Variability and Its Impact on Advanced Process Technologiesand Product Design"** (4:00pm-6:00pm) - *Professor Asen Asenov*, James Watt Professor in Electrical Engineering, Glasgow University (Presentation 3.4)

# SICTW Program (November 9th)

- **"Segmented Channel Design to Extend Planar Bulk MOSFET Technology Roadmap"** (8:30am-10:30am) – *Dr. Nuo Xu,* Research Scientist, Samsung US Headquarter – Device Solutions, and *Professor Tsu-Jae King Liu,* TSMC Distinguished Professor in Microelectronics in Electrical Engineering & Computer Sciences, and Vice Provost for Academic and Space Planning, University of California at Berkeley (Presentation 4.1)
- Break (15 minutes)
- **"FDSOI Technology for Ultra-Low Power Products"** (10:45am-12:45pm) – *Dr. Olivier Weber,* CEA-Leti, MINATEC Campus, GRENOBLE, France (Presentation 4.2)
- Lunch (12:45pm-2:00pm)
- **"CAD Based DTCO"** (2:00pm-4:00pm) – *Dr. Victor Moroz*, Synopsys Fellow, and *Professor Asen Asenov*, James Watt Professor in Electrical Engineering, Glasgow University (Presentation 4.3)
- Break (15 minutes)
- **"Process Design Kit for Nanometer Technologies"**(4:15pm-5:45pm) – *Dr. Waisum Wong*, manager of Technology Design Enablement Team, HiSilicon, Huawei (Presentation 4.4)
- Farewell and closing remarks by workshop organizer (5 minutes)

# On to the Next Fifty Years – Guideposts from the Past Fifty Years



**Professor H.-S. Philip Wong, Willard R. and Inez Kerr Bell Professor**
**Department of Electrical Engineering and Stanford SystemX Alliance, Stanford University, Stanford, California**

**Abstract:** Far from signaling an end to progress, the gradual end of Moore's law will open a new era in information technology as the focus of research and development shifts from miniaturization of long-established technologies to the coordinated introduction of new devices, new integration technologies, and new architectures for computing. The quest for better computing is best summarized by the grand challenge for future computing announced by the White House Office of Science and Technology Policy, aiming to "create a new type of computer that can proactively interpret and learn from data, solve unfamiliar problems using what it has learned, and operate with the energy efficiency of the human brain."

If history can serve as a guide, the advances in the past five decades may help us chart a new course for the next fifty years. In this talk, I will review some of the important advances in semiconductor devices and device fabrication that occurred in the past fifty years. I will also highlight the commonalities and differences between our past experiences and the new technology landscape that we will live in.

Acknowledgements: This work is supported in part by member companies of the Stanford SystemX Alliance, the National Science Foundation (E2CDA, Expeditions in Computing), and also in part by Systems on Nanoscale Information fabriCs (SONIC) and Center for Function Accelerated nanomaterial Engineering (FAME), two of the six SRC STARnet Centers, sponsored by MARCO and DARPA.

**Biography:** *H.-S. Philip Wong* is the Willard R. and Inez Kerr Bell Professor in the School of Engineering. He joined Stanford University as Professor of Electrical Engineering in September, 2004. From 1988 to 2004, he was with the IBM T.J. Watson Research Center. At IBM, he held various positions from Research Staff Member to Manager and Senior Manager. While he was Senior Manager, he had the responsibility of shaping and executing IBM's strategy on nanoscale science and technology as well as exploratory silicon devices and semiconductor technology. Professor Wong's research aims at translating discoveries in science into practical technologies. His works have contributed to advancements in nanoscale science and technology, semiconductor technology, solid-state devices, and electronic imaging. He is a Fellow of the IEEE. He served as the Editor-in-Chief of the IEEE Transactions on Nanotechnology (2005 – 2006), sub-committee Chair of the ISSCC (2003 – 2004), General Chair of the IEDM (2007), and is currently the Chair of the IEEE Executive Committee of the Symposia of VLSI Technology and Circuits. He is the founding Faculty Co-Director of the Stanford SystemX Alliance – an industrial affiliate program focused on building systems.

# China's IC Industry:
# Current State, Environment and Opportunities During Post Moor's Era

**Dr. Hanming Wu**
**CEO of BrightIP and Consultant to SMIC**

**Abstract:** The IC industry is one of the most critical factors to national economic development. Not only because of its sheer economic volume, but also it is foundation to almost all areas of the national economy. Therefore, all governments around the world devote significant amount of attention to promote IC industry. However, rapid development of IC industry is blocked by the following factors: 1) Wide industry chain and related areas; 2) Intensified capital investment; 3) Extreme technological complexities.

It is well known that China had become the largest IC market as well as the largest IC product importing country in the world. More than $230 Billion IC products import to China in 2016 alone. For economic reasons, it is imperative for China to enhance its entire domestic IC industry's eco-system to realize a significantly larger portion of its IC demand be contributed from its domestic production. National security in communication is another important objective.

In this talk, the history, the current state, the China environment and challenges as well as the enormous opportunities will be presented and discussed, including foundries, fabless design houses, equipment manufacturers, material suppliers, industry-university-institute alliances, etc.

**Biography:** Dr. Wu received his PhD degree from the Chinese Academy of Sciences in 1987 and was elected to Research Professor at the same institute in 1989. Subsequently, he conducted postdoctoral research at UT-Austin and UC-Berkeley. He also has extensive R&D experiences in the US semiconductor industry, first at Novellus and then at Intel until 2000. He joined SMIC in 2001 and was instrumental in setting up R&D team for etch process. As a leader on the national project《65-45-32nm Process Technology Development》, he initiated the national 65-32nm CMOS pre-manufacture projects. As VP of SMIC's R&D, Dr. Wu played a key role in SMIC's path finding activities during 2012-2015. He had published more than 100 papers and is the inventor on more than 80 granted patents on semiconductor processes. In 2015, he started a new company BriteIP with specialty in IP platform for design houses.
As a conference chair in 2010-2011, he successfully led CSTIC in becoming the largest semiconductor technology conference in China. He was also a conference co-chair of ISTC 2008-2009 and CSTIC2012-2017. He has earned three National 2nd Level Awards for Advanced Technology Achievement. He was elected as "*2014 The Best National Ten Excellent Scientists*" and "*2014 National Outstanding Talent of Specialty*". He was also selected to be "Beijing Scholar". He has been a member of the National Expert Group for the 02 National Key Projects since 2009.

# Nanometer IC Design and Process Technology Co-Optimzations – Challenges and Practices

**Professor David Z. Pan, Engineering Foundation Endowed Professor**

**Department of Electrical and Computer Engineering, University of Texas at Austin, TX**

**Abstract:** As the semiconductor industry enters the era of extreme scaling, IC design and manufacturing challenges are exacerbated, which calls for increasing design and technology co-optimization (DTCO). DTCO requires cross-layer information feed-forward and feed-back, to enable the overall design and manufacturing closure and optimization. This talk will present some key challenges and practices how to enable such DTCO, from mask synthesis, to standard cell design, and to physical design. Some topics which will be covered include: design-intent aware layout decomposition under multiple patterning lithography (MPL), machine learning based lithography hotspot detection and mask/physical synthesis, standard cell pin access and routing optimizations, MPL aware placement, etc. As new process technologies being proposed (e.g., new transistor structures, new materials) and new design requirements (e.g., reliability and security) popping up, we expect to see many new opportunities for synergistic design and process technology co-optimizations.

**Biography:** David Z. Pan received his BS degree from Peking University in 1992, and his PhD degree in Computer Science from UCLA in 2000. He was a Research Staff Member at IBM T. J. Watson Research Center from 2000 to 2003. He is currently a full professor and holder of the Engineering Foundation Endowed Professor #1 at the Department of Electrical and Computer Engineering, University of Texas at Austin. He has published over 290 refereed journal/conference papers and 8 US patents, and graduated over 20 PhD students. He has served in many premier journal editorial boards and conference committees, including various leadership roles. He has received a number of awards, including the SRC Technical Excellence Award, 14 Best Paper Awards, DAC Top 10 Author Award in Fifth Decade, ASP-DAC Frequently Cited Author Award, Communications of ACM Research Highlights, ACM/SIGDA Outstanding New Faculty Award, NSF CAREER Award, NSFC Overseas and Hong Kong/Macau Scholars Collaborative Research Award, SRC Inventor Recognition Award three times, IBM Faculty Award four times, UCLA Engineering Distinguished Young Alumnus Award, UT Austin RAISE Faculty Excellence Award, many international CAD contest awards, among others. He is a Fellow of IEEE and SPIE.

# Advanced Lithography and Patterning Technologies For and Beyond 5nm

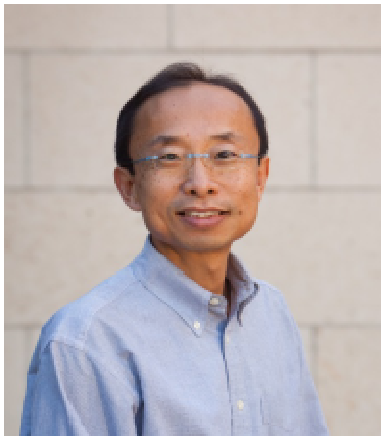
**Dr. Yan Borodovsky, Former Intel Sr. Fellow & Director of Lithography**

**Abstract:** For over 50 years Semiconductor Industry ecosystem supported high volume manufacturing of ICs that followed famous Gordon Moore's exponential transistors density and cost rate of change prediction. Yet, resolution and printed dimensions control of Lithography Exposure tools used in High Volume Manufacturing were and are lagging IC patterning needs as demanded by economy of Moore's Law for last 20+ years. As a result, ever more complex patterning techniques that result in additional wafer cost were introduced at every node driving inter node wafer cost growth from traditional 10% to 30% or more. This in turn resulted in need for significant change in approach to IC design layout rules, higher capital equipment reuse rates, significant change in CAD and Mask Making equipment and other important changes to wafer and mask making infrastructure.Due to complex relations between patterning costs currently reaching 50% of total wafer costs and device design rules, device architecture, various and different sets of imaging, etching, thin films and CAD tools and materials needed to support various routes of wafers processing Integrated Device Manufacturers and Foundries face difficult choices in managing R&D resource allocation capable to identify optimal strategy for 5nm node and beyond IC production that will continue historical trend of inter node IC area density growth and cost per transistor reduction.

Presentation will start with short "Lithography Primer" to stage the scene for discussion of key factors that influence selection of particular tools and materials sets for technology node under development to be followed by talk on what, in author opinion, are critical factors and innovative patterning approaches to enable progression of Moore's Law to and beyond 5nm Node.EUV readiness to support future nodes High Volume Manufacturing, barriers to its insertion and competing technological approaches will be discussed in some details as EUV continue to dominate discussions involving patterning options for future technology nodes. Talk will conclude with substantial Q&A portion intended to clarify, if necessary, concepts presented as well as to answer any pertinent technology questions.

**Biography:** Yan received his MS in Solid State devices from Tula Polytechnic in 1971. Upon coming to California, he worked at Syncal Corporation during 1979-1982 developing semiconductor thermoelectric conversion materials for deep space satellites power supplies. He started his career as a lithographer at AMD in 1982 and in 1985 joined ATEQ to develop optical path design and assembly, optics test stand and resist process for CORE 2000 laser writer. Yan joined Intel in 1987. During the 28 years at Intel, Yan worked on all aspects of Intel Lithography and led Intel Lithography Roadmap development, numerous novel lithography processes, tools and materials Pathfinding and Development as well as process-design co-optimization that enabled Intel leadership position for multiple technology nodes from 0.5micron to 7nm node when he retired in 2015. Yan is author of many US patents, publications and presentations at key Lithography Forums. Yan's contributions to Intel were recognized by appointment to Intel Fellow in 1999 and to Intel Sr. Fellow in 2003. His fundamental contributions were recognized by the industry via his election to SPIE Fellow in 2013 and the recipient of IEEE Cledo Brunetti Award in 2012 "For developing and implementing innovative lithographic and patterning equipment and processes to enable cost-effective scaling for logic technologies." In 2016 SPIE awarded Yan prestigious annual Frits Zernike Award "in recognition of his efforts toward the advancement of multi-generational lithography process solutions and as a key contributor of patterning approaches and layout design rules at Intel.

# Reaching for the N3XT 1,000× of Computing Energy Efficiency



**Professor H.-S. Philip Wong, Willard R. and Inez Kerr Bell Professor**
Department of Electrical Engineering and Stanford SystemX Alliance, Stanford University, Stanford, California

**Abstract:** 21st century information technology (IT) must process, understand, classify, and organize vast amount of data in real-time. 21st century applications will be dominated by memory-centric computing operating on Tbytes of *active* data with little data locality. At the same time, massively redundant sensor arrays sampling the world around us will give humans the perception of additional "senses" blurring the boundary between biological, physical, and cyber worlds. Abundant-data processing, which comprises real-time big-data analytics and the processing of perceptual data in wearable devices, clearly demands computation efficiencies well beyond what can be achieved through business as usual.

The key elements of a scalable, fast, and energy-efficient computation platform that may provide another 1,000× in computing performance (energy-execution time product) for future computing workloads are: massive on-chip memory co-located with highly energy-efficient computation, enabled by monolithic 3D integration using ultra-dense and fine-grained massive connectivity. There will be multiple layers of analog and digital memories interleaved with computing logic, sensors, and application-specific devices. We call this technology platform N3XT – Nanoengineered Computing Systems Technology. N3XT will support conventional computing architectures as well as computation methods that embrace sparsity, stochasticity, and device variability, including those that are neuromorphic and learning-based.

In this talk, I will give an overview of nanoscale memory and logic technologies for implementing N3XT. I will give examples of nanosystems that have been built using these technologies, and provide projections on their eventual performance.

**Biography:** *H.-S. Philip Wong* is the Willard R. and Inez Kerr Bell Professor in the School of Engineering. He joined Stanford University as Professor of Electrical Engineering in September, 2004. From 1988 to 2004, he was with the IBM T.J. Watson Research Center. At IBM, he held various positions from Research Staff Member to Manager and Senior Manager. While he was Senior Manager, he had the responsibility of shaping and executing IBM's strategy on nanoscale science and technology as well as exploratory silicon devices and semiconductor technology. Professor Wong's research aims at translating discoveries in science into practical technologies. His works have contributed to advancements in nanoscale science and technology, semiconductor technology, solid-state devices, and electronic imaging. He is a Fellow of the IEEE. He served as the Editor-in-Chief of the IEEE Transactions on Nanotechnology (2005 – 2006), sub-committee Chair of the ISSCC (2003 – 2004), General Chair of the IEDM (2007), and is currently the Chair of the IEEE Executive Committee of the Symposia of VLSI Technology and Circuits. He is the founding Faculty Co-Director of the Stanford SystemX Alliance – an industrial affiliate program focused on building systems.

# Time-to-Market Minimization for New Product Introduction in Leading Edge Technology Nodes

**Professor Andrzej J. Strojwas, Joseph F. & Nancy Keithley Professor of Electrical & Computer Engineering,**
**Carnegie Mellon University and Chief Technologist, PDF Solutions, Inc.**

**Abstract:** With the introduction of FinFETs, the technology complexity has increased so significantly that bringing up new products has become extremely challenging. The number of design rules has been growing exponentially and the layout patterns introduced by different lead products force the co-optimization of the technology and product design. This is especially true for the 7nm node which has been introduced without EUV lithography and thus requires multiple patterning at all critical layers. Major reasons for yield loss have also evolved, and the systematic and parametric yield losses now dominate. In this lecture, I will present the key challenges that are faced by the leading edge foundries and fabless companies to minimize the time-to-market for the leading edge products and present solutions that have proven to be effective. We will start by describing a methodology for achieving robust design rules by deploying comprehensive characterization vehicles. Next, we will introduce the concept of *Templates* which are the quantized legal layout shapes and locations within pre-defined cell images that have replaced the free form rule based layout in order to maximize pitch scaling. Selecting the optimal limited set of layout patterns that are used in a given *Template* is the new essence of Design For Manufacturability (DFM). These layout patterns need to be chosen to account for circuit needs as well as to navigate process variability sources. Process variability needs to be characterized in silicon to identify the layout patterns with sufficient process margin. Device scaling and the application of stressors in modern device architectures require exhaustive silicon characterization of transistor behavior. Device modeling had to shift to focus upon the characterization of a specific limited set of transistor layout patterns and neighborhoods, rather than general purpose models that span a broad rule space. We will demonstrate techniques for exhaustive characterization of the parametric variations of transistor behavior by deploying specially designed characterization vehicles before product design, as well as verifying their performance by the *direct probe* measurements of all layout patterns in the actual product die made possible by the deployment of a massively parallel tester. If executed properly, this will enable fabless and foundries to eliminate the months or in some cases years of physical debug efforts that have plagued lead product ramps at advanced nodes. Characterizing the complex yield loss reasons has become almost mission impossible since, on top of hard failures such as shorts or opens, the soft failures such as leakages and soft opens (e.g., resistive contacts/vias) are even more difficult to detect and they are most often systematic in nature due to specific layout patterns very often related to the extremely difficult to meet process window or alignment tolerances in the multiple patterning schemes. Traditional optical inspection schemes are unable to detect these often invisible defects and the typical e-beam tools are far too slow to detect these failures. We will present a novel technique called *Design For Inspection* (DFI) that has been introduced to provide a time and cost effective characterization of these failures. The DFI cells are designed to be sensitized to a specific failure mode thus allowing for precise location and identification of the failure mechanism. These DFI cells are inserted either in the scribe areas or in the actual product die in place of filler cells and dummy fill and then inspected by the custom-made e-beam tool which is capable of contact-less inline inspection of several billions of these cells per wafer in a couple of hours. We will demonstrate all the above described techniques by the actual examples from the 16/14, 10 and 7nm processes.

**Biography:** ANDRZEJ J. STROJWAS is Joseph F. and Nancy Keithley Professor of Electrical and Computer Engineering at Carnegie Mellon University. Since 1997 he has served as Chief Technologist at PDF Solutions, Inc. He has held positions at Harris Semiconductor Co., AT&T Bell Laboratories, Texas Instruments, NEC, HITACHI, SEMATECH, KLA-Tencor and PDF Solutions, Inc. He received multiple awards for the best papers published in the IEEE *Transactions on Computer-Aided Design of Integrated Circuits and Systems*, *IEEE Transactions on Semiconductor Manufacturing* and IEEE-ACM Design Automation Conference. He is also a recipient of the SRC Inventor Recognition Award. He was the Editor of the IEEE *Transactions on CAD of ICAS* from 1987 to 1989. He served as Technical Program Chairman of the 1988 ICCAD and Conference Chairman of the 1989 ICCAD. He has graduated almost 50 PhD students and has authored or co-authored 15 books/book chapters, and more than 350 papers in the leading journals or technical conferences. In 1990 he was elected IEEE Fellow. In 2016 he received the Electronic System Design Alliance Phil Kaufman Award for his pioneering and sustained contributions to Design for Manufacturing.

# Computational Imaging: Scaling Walls

**Dr. Vivek Singh, Intel Fellow & Director of Computational Imaging**

**Abstract:** Moore’s Law is an observation that a transistor – the fundamental building block of the digital age – will decrease in cost at a steady, exponential rate. This decrease in cost as well as transistor size over the past 50 years has also led to dramatic increases in compute power and energy efficiency and transformed our world with ever-more powerful smart phones, tablets, personal computers and data centers. While industry observers continue to predict that Moore’s law will hit a wall, motivated teams continue to find innovative solutions to scale these walls. Many of the challenges and innovations that enable Moore’s Law scaling are in the field of imaging and mask manufacturing. This paper will describe some of those challenges and associated opportunities, with a particular focus on two facets of Computational Imaging: Inverse Lithography, and Smart Metrology. Inverse lithography enables better utilization of the resolution capability of lithography tools and masks. Smart metrology enables rapid identification of defects, buried like needles in gigantic haystacks of manufacturing data. These two fields require deep knowledge of such esoteric fields as diffractive optics, as well as prove to be fertile grounds for emerging techniques in Artificial Intelligence. Such innovations, fed by a rich technology pipeline, give us confidence that Moore's Moore's Law will continue.

**Biography:** Vivek Singh is an Intel Fellow in the Technology and Manufacturing Group, and Director of Computational Imaging in Logic Technology Development. He is responsible for Intel's software development in full chip OPC, lithography verification, rigorous lithography modeling, next-generation lithography selection, inverse lithography technologies, image processing, smart metrology for yield, and Big Data and AI techniques in Technology Development. He is an SPIE Fellow, and the current President of the Lithography Workshop. Singh joined Intel in 1993 as a modeling applications engineer, was appointed leader of the Lithography Modeling Group in 2000, and was named an Intel Fellow in 2008. He holds 30 patents and has published over 50 technical papers. Singh graduated from the Indian Institute of Technology in Delhi with a bachelor's degree in chemical engineering in 1989. He earned a master's degree in chemical engineering in 1990, a Ph.D. minor in electrical engineering in 1993, and a Ph.D. in chemical engineering in 1993, all from Stanford University.

# Is the FINFET finished?
# -- Challenges of 10 nm and 7 nm FINFET for Server and Mobile Applications

**Dr. Rama Divakaruni**
**IBM Distinguished Engineer, IBM Advanced Process Technology Research**

**Abstract:** CMOS scaling has served the semiconductor industry and transformed the world exceedingly successfully over the past several decades. In recent times, the transition to hi-K dielectric interfaces enabled CMOS to shrink circuits to below the 32nm node. The advent of fully depleted devices (FDSOI, FINFETs) have enabled CMOS scaling to the limits of conventional 193nm optical immersion lithography over the past decade, CMOS scaling has transformed mobile technologies. The cell phone and smartphone have become ubiquitous as increased performance has been garnered to increase functionality on the form factor at constant power (Watt regime). The resulting boom in data has transformed industries and fueled the social network and the "app" world. 14nm and 10nm FINFET bulk technology is now available on cutting edge mobile devices. The 10nm and 7nm nodes will see various incarnations across the major semiconductor fabricators. The pressure on density to reduce cost will result in the adoption of multiple patterning techniques for the FIN, Gate and various Middle Of Line (MOL) and Back End Of Line (BEOL) wiring levels. The need to reduce doping in the FINFETs will result in Multi-Workfunction-Gates. Novel materials will be needed to reduce parasitic capacitance and resistance in the MOL and BEOL levels. Some incarnations of the 10nm node will be called "7nm", but the true "7nm" node circuit densities will require the next generation of lithography -- Extreme Ultra Violet (EUV) at 13.6nm wavelength. The key to adoption in the commoditized mobile space is thus the cost of the chip which is challenged by the need for novel cost intensive patterning techniques and new materials. While power and form factor are key to the mobile world, Server applications have required performance at much higher power (100+ Watt regime). CMOS scaling has served this market very well over the decades as improved transistors have always been utilized for increased performance (high end servers run > 5 GHz). The growth in the server market has migrated to large datacenters for cloud applications and away from standard transaction processing (which still remains important in many areas). This market is served predominantly by 14nm bulk and SOI FINFETs. Parasitic components on FINFETs are thus much more critical in this market and has thus driven early adoption of "next generation" materials and processes. The adoption of 10nm and 7nm nodes in this space will be determined less by cost than by ability to get better performance at constant chip power given the increased parasitics in the MOL and BEOL. This drives the need for introduction of new novel materials for improved performance and reliability.

**Biography:** Rama Divakaruni received B.Tech in Electrical Engineering from Indian Institute of Technology, Madras in 1988. He received PhD in Electrical Engineering at UCLA in 1994. Since 1994, he has been working on advanced semiconductor technologies at IBM. From 1994 through 2003, he worked in DRAM Technology Development and his team introduced the world's first sub-8F2 vertical transistor DRAM trench technology. From 2004 through 2006 he worked as the technical lead for the 90nm strained silicon technology which was the world's first to introduce dual stress liner technology. This technology was the basis of the Nintento Wii, XBOX360 and the PlayStation3 game platforms. After a year serving as the project manager for the Unit Process team, Dr. Divakaruni served as the program manager and technical lead for the development of 45nm industry standard bulk technologies for IBM's Joint Development Alliance. At 45nm, IBM and its development partners introduced strained silicon technology for low power mobile products thus introducing strained silicon across the spectrum of bulk low power and SOI performance CMOS technologies. This technology was the basis for the first Apple I-pad, early Apple I-phones and was the technology that IBM's partners including Samsung used for all their mobile platforms and devices. From 2008 through 2010, Dr. Divakaruni worked on IBM's unique Gate 1st Hi-K technology, which is the bedrock of the 32/28nm technologies from the IBM partnership across Global Foundries, Samsung and STMicroelectronics. He has since served at the IBM Alliance Chief technologist for the CMOS JDAs. Dr. Divakaruni is currently an IBM Distinguished Engineer and is responsible for IBM Advanced Process Technology Research (which includes EUV technologies and advanced unit process and Enablement technologies needed for transistors beyond 7nm FINFETs (i.e Nanosheets and Vertical Transistors)) as well as main interface between IBM Semiconductor Research and IBM's Systems Leadership. He is one of IBMs top inventors with over 225+ issued US patents.

# Interconnect - the Past, the Present and the Future

**Dr. Mehul Naik**
**Principal Member of Technical Staff, Applied Materials**

**Abstract:** We will take a comprehensive view at the evolution of the Interconnect over the last 20 years, starting from the revolutionary change of the conductor from Aluminum to Copper in the 90's, then the demanding transition from oxides and fluorine doped oxide insulators to carbon doped oxides in the early 2000's, to the use of CVD Co liner and selective CVD Co cap at 20nm node and implementation of air-gap at 14nm node. We will review the impetus for these changes, challenges faced and solutions developed. As we move beyond the state of the art production device at 10nm node, interconnect resistance now becomes a key bottleneck which can effectively negate all the great engineering effort and innovations in the device architecture. New materials or new process technologies or modified process flows or all of them in one combination or other maybe required to manage interconnect resistance. We will see how the interconnect roadmap is expected to evolve as the industry prepares for 7nm node and develops the technology pieces required to enable 5nm node.

**Biography:**Dr. Mehul Naik is a Principal Member of Technical staff with the Advanced Product Technology Development team in the Transistor and Interconnect Group at Applied Materials. He is responsible for the Interconnect Program and serves as a cross-functional owner of Applied's interconnect roadmap. He has authored over 45 publications and holds over 50 U.S patents on various topics including Cu and alternate metallization, CMP, selective deposition, process flows, low k integration, and double patterning. He serves on the North American Program Committee for the International Interconnect Technology Conference (IITC), and also as an executive committee member for the Advanced Metallization Conference (AMC). Mehul holds a Ph.D. in Chemical Engineering from Rensselaer Polytechnic Institute.

# Variability and Its Impact on Advanced Process Technologies and Product Design

**Professor Asen Asenov**
**James Watt Professor in Electrical Engineering, Glasgow University**

**Abstract:** The variability is the maker or breaker of advanced CMOS technology and one of the major challenges in developing new technology generations including, Bulk, FDSOI and FinFET based CMOS. In this lecture we will provide a systematic classification of the different types of CMOS variability including long-range process induced variability and short-range statistical variability introduced by the discreteness of charge and granularity of matter. In particular, we will focus on the different sources of short-range statistical variability including random discrete dopants, line edge roughness and metal gate granularity. We will introduce also the time dependent variability associated with the progressive discrete charge trapping in the gate dielectric. We will describe how the long-range process induced variability and the short range statistical variability and their interactions can be captured in advanced TCAD simulation and in compact models suitable for circuit design and verification. We will illustrate how the variability can be captured in early PDK development and in TCAD based DTCO. We will elaborate how the different types of CMOS variability affect the logic and memory design, and how their impact can be capture and mitigated in circuit simulation and validation level. Example of advanced bulk, FDSOI and CMOS technologies will be provided.

**Biography:** Professor Asen Asenov (Fellow of IEEE, Fellow of Royal Society of Edinburgh) is the James Watt Professor in Electrical Engineering and the Leader of the renown Glasgow Device Modelling Group directs the development of quantum, Monte Carlo and classical models and tools and their application in the design of advanced and novel CMOS devices. He also was founder and the CEO of Gold Standard Simulations (GSS) Ltd. After the acquisition of GSS in 2016 by Synopsys he shares his time between Glasgow University and Synopsys.

# Segmented Channel Design to Extend Planar Bulk MOSFET Technology Roadmap

*Dr. Nuo Xu*, Research Scientist
Samsung US Headquarter – Device Solutions

TSMC Distinguished Professor in Microelectronics in
Dept. of Electrical Engineering & Computer Sciences, and Vice Provost for Academic and Space Planning, UC Berkeley

**Abstract:** The constant pitch scaling of CMOS technology has sustained during the past decades to ensure the continuous cost reduction and performance improvement of integrated circuits. As transistor's gate lengths are scaled below 30nm, electrostatic integrity and process-induced variability become harder to control. To mitigate these issues, transitions from conventional planar bulk MOSFET to revolutionary thin-body structures such as FinFET and fully-depleted SOI (FDSOI) MOSFET have taken place. However, these advanced technologies require substantially increased process complexity and more expensive substrate costs. As for certain applications (such as mobile and Internet-of-Things, IoT), cost is an important factor, indicating the opportunities to extend planar bulk like transistors as a competitive alternative. A segmented channel MOSFET (SegFET) design combines the benefits of both low-cost heritages from planar channels and improved electrostatic integrity from thin-body structures, providing an evolutionary way to enable planar bulk MOSFETs scale below 20nm. In this tutorial, details regarding fabrication flow for corrugated substrate and device performance study for SegFETs will be discussed. Experimental results comparing SegFET and its planar counterpart will be presented to show its capability to suppress short-channel effects while achieving comparable or better ON-state current. TCAD simulations further benchmarked SegFET with FinFET designs, suggesting potential advantages due to comparable DC while better AC performances (less parasites) in SegFETs. Much less aggressive retrograde channel doping gradient is needed in SegFETs as compared to other bulk transistors (planar and fin) to ensure good manufacturability. High-mobility channel materials (*i.e.* strained $Si_{1-x}Ge_x$) are also implemented into SegFETs and demonstrated for superior analog/RF performance metrics, making SegFETs promising for System-on-Chip (SoC) applications. The design guidelines for SegFET scaling is provided at the end of this talk to offer a viable and healthy pathway to broaden the semiconductor technology roadmap.

**Biography:** Dr. Nuo Xu received the B.S. (2008) degree from Peking University and M.S. (2010) and Ph.D. (2012) degrees from University of California at Berkeley, all in Electrical Engineering. He has been with Synopsys Inc., Mountain View, CA and IMEC, Heverlee, Belgium during 2010 and 2011. From 2012 to 2014, he was a visiting faculty and post-doctoral scholar at UC Berkeley. In 2014 he joined Samsung US Headquarter - Device Solutions, San Jose, CA and is currently a staff research scientist. Dr. Xu's research interests include the development of emerging semiconductor technologies, such as transistors, non-volatile memories and MEMS devices, as well as applying deep learning algorithms to Electronic Design Automation (EDA) and implementing these algorithms at a hardware level. He has published over 70 technical papers on journals and conferences, and has 10 US Patents granted or under application. Dr. Xu received multiple awards from IEEE Electron Device Society and industry, and has served in technical program committees for conferences such as IEEE SOI/S3S and VLSI-TSA, *etc*.

**Biography**: Professor Tsu-Jae King Liu received the B.S., M.S., and Ph.D. degrees in Electrical Engineering from Stanford University. From 1992 to 1996 she was a Member of Research Staff at the Xerox Palo Alto Research Center (Palo Alto, CA). In August 1996 she joined the faculty of the University of California, Berkeley, where she currently holds the TSMC Distinguished Professorship in Microelectronics in the Department of Electrical Engineering and Computer Sciences, and also serves at the campus level as Vice Provost for Academic and Space Planning. Dr. Liu's research contributions in the area of semiconductor devices and technology include the DARPA Significant Technical Achievement Award (2000) for development of the FinFET, the IEEE Kiyo Tomiyasu Award (2010) for contributions to nanoscale MOS transistors, memory devices, and MEMs devices, the Semiconductor Industry Association Outstanding Research Award (2014), and the Semiconductor Research Corporation Aristotle Award (2016). She is a Fellow of the IEEE and a member of the U.S National Academy of Engineering.

# FDSOI Technology for Ultra-Low Power Products

**Dr. Olivier Weber**

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**Abstract:** The IoT (Internet of Things) market demand for low cost, low leakage and energy efficient technologies is relentless. First introduced at the 28nm node [1], and developed later at 22nm [2] and 14nm nodes [3] as a low-cost alternative to FinFET [4], the FDSOI technology has many assets allowing to respond to this demand. A 65nm node version of this technology [5] has been also developed for IoT applications purpose.This lecture will be divided in four parts. Part I will expose some fundamentals of the FDSOI devices, highlighting the importance of the electrostatic control in advanced CMOS devices. The FDSOI device construction will be presented in part II. In particular, the way to achieve multiple VTs device will be extensively described. The main specific process features of this technology will be covered in part III including: (1) The hybrid integration allowing the co-integration of bulk devices, (2) SiGe channel formation, (3) Gate stack engineering, (4) Raised source-drain epitaxy.Finally, in part IV, it will be highlighted how the FDSOI device, with its specific differentiating features over bulk and FinFET technologies, has become the most suitable device for ultra-low power and IoT products. The most added value of this device comes from the back bias technique that can serve to drastically boost the energy efficiency or to mitigate the leakage. Low parasitic gate capacitance, low VT mismatch associated with its undoped channel, and low gate resistance linked to the gate-first integration also bring some competitive advantages to FDSOI over FinFETs for Analog and RF devices.

**Biography:** During his Ph.D. studies, between 2002 and 2005, he worked at CEA-LETIin France on fabrication and characterization of advanced CMOS transistors featuring strained-Si and Ge channels and high-k/metal gate stacks. In 2006 and 2007, he was a Postdoctoral Fellow at University of Tokyo engaged in research on the physics and characterization of strained-Si MOS devices with Professor S. Takagi. Between 2008 and 2010 at CEA-LETI, Grenoble, he worked in advanced device group on FDSOI CMOS technology. He moved in 2011 to STMicroelectronics for starting 28nm FDSOI platform, in charge of device construction and integration. Next, he moved to the 14nm FDSOI group in its early phase of development in 2012, in charge of the device platform construction and device & SRAM integration. Since 2016, he is working on phase change memory device/design in the eNVM 28nm FDSOI group.He is author or coauthor of more than 100 publications, including 5 IEDM and 7 VLSI Technology Symposium publications as first author. He holds more than 10 patents in the field of CMOS integration and device. He served as a committee member of the international symposium on VLSI Technology, Systems and Applications (VLSI-TSA) and of the Solid-state device and materials (SSDM) conference since 2009.

# CAD Based DTCO

**Dr. VictorMoroz**
**Synopsys Fellow**

**Professor Asen Asenov**
**James Watt Professor in Electrical Engineering, Glasgow University**

**Abstract:** Design-Technology Co-Optimization (DTCO) has become mandatory in advanced technology nodes. It is well understood that tailoring the transistor characteristics by tuning the technology is not sufficient any more. The transistor characteristics have to meet the requirement for design and optimization of particular circuits, systems and corresponding products. Modeling and simulation play an increasing important role in the DTCO process with the benefits of speeding up and reducing the cost of the technology, circuit and system development and hence reducing the time-to-market. In particular fin depopulation has been instrumental in decreasing power density and enabling library height reduction down to 6 tracks. Transition to 5 tracks will likely require a single fin design, which is friendly to NCFET, isolating gates, and electromigration, but is more exposed to variability. It is clear that round nanowires have too many issues that morph them into some version of a nano-slab that is essentially “a fin that lays down on its side”. There’s a limit to how narrow the fin can be (and correspondingly how thin a nano-slab can be) before band structure fluctuations due to atomic steps on the surface take over. The competition between ultimately scaled FinFETsand nano-slabs will be mainly in terms of manufacturing variability and MOL capacitance instead of the initially anticipated differences in scaling potential.
In this paper we will present advanced tools and toll flows developed by Synopsys to enable TCAD based DTCO. Two DTCO flavors will be discussed in details: (1) **Path Finding DTCO** which facilitates the screening of different material and transistor architecture options for future CMOS technology generations saving significantly the research costs and facilitating the decision making by foundries, IDMs and fables design companies; (2) **Pre Wafer DTCO** which reduces the technology development costs and time to market and allows the development of accurate pre-silicon PDKs.
In particular, we will review all intricate aspects of 5nm/3nm/2nm technology based on different analysis techniques, ranging from band structure to manufacturability and Power-Performance-Area benchmarking.

**Biography:** Dr. Victor Moroz grew up as a hunter-gatherer in Siberia and received M.S. degree in Electrical Engineering from Novosibirsk Technical University and Ph.D. degree in Applied Physics from the University of Nizhny Novgorod. After engaging in technology development at several semiconductor manufacturing companies and teaching semiconductor physics at a University, Dr. Moroz joined a Stanford spin-off Technology Modeling Associates in 1995. After IPO in 1997, the TMA TCAD team became part of Avanti in 1998, and in 2002 it became a key part of Synopsys, connecting a synthesis company to the manufacturing. Currently Dr. Moroz is a Synopsys Fellow, engaged in a variety of projects on modeling advanced CMOS with over 100 granted and pending US patents, and serving as an Editor of IEEE Electron Device Letters.

**Biography:** Professor Asen Asenov (Fellow of IEEE, Fellow of Royal Society of Edinburgh) is the James Watt Professor in Electrical Engineering and the Leader of the renown Glasgow Device Modelling Group directs the development of quantum, Monte Carlo and classical models and tools and their application in the design of advanced and novel CMOS devices. He also was founder and the CEO of Gold Standard Simulations (GSS) Ltd. After the acquisition of GSS in 2016 by Synopsys he shares his time between Glasgow University and Synopsys.

# Process Design Kit for Nanometer Technologies

**Dr. Waisum Wong**

**Manager of Technology Design Enablement Team, HiSilicon**

**Abstract:** This presentation will cover the basic analog design flow and the introduction of PDK package for the analog designs. Attendees will learn the basic PDK platforms currently available in IC industry. Since PDK package contains Pcell lib, DRC runset, LVS techfile, RCX techfile, and utilities, detail introduction for each of these areas will be presented. Physical design requires the understanding of basic process knowledge and constraint, therefore LDE will be described in this lecture. For the advanced Finfet technology layout dependent effects can be addressed through PDK to either make use of or avoid them during the physical design. RC extraction is so important for the advanced node and it demands special attention. RC tech file should attend high level of accuracy with highest efficiency to meet design requirements. We also present a flow of how to qualify a incoming PDK, RCX, as a user. We will provide our perspective as how a future PDK will trend, such as addressing the SHE/EM, aging, within PDK, and creating template based Pcell for design. In summary the attendees will have an overview of analog design flow, what is PDK, how PDK works, how to perform QA of a PDK for the advanced node.

**Biography:** Dr. Wong is currently working at Huawei and responsible for the Technology Design Enablement (TDE) Team supporting PDK, compact models, process reliability and design for reliability. Prior to working at Huawei, he had worked at Qualcomm, Intel, EXAR and Siliconix in the US and SMIC in Shanghai during the past 26 years. Dr. Wong has extensive experience in device design, device reliability, device modeling and characterization, and PDK development. He has coauthored two books and published over 50 papers. He is also the owner of numerous patents in US and China.